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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Kaushik Saha

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SUITE 350

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EXAMINER

DO, CHAT C

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/781,336	<b>Applicant(s)</b> SAHA ET AL.	
	<b>Examiner</b> Chat C. Do	<b>Art Unit</b> 2193	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2009 and 15 June 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-8 is/are allowed.
- 6) ☒ Claim(s) 1,2,9-13,16,17 and 20-23 is/are rejected.
- 7) ☒ Claim(s) 3,4,14,15,18 and 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>07/06/2009 and 06/15/2009</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This communication is responsive to Amendment filed 04/13/2009, 06/15/2009 and 07/06/2009.
2. Claims 1-23 are pending in this application. Claims 1, 5, 9, 16 and 21 are independent claims. This Office Action is made non-final after a RCE filed 06/15/2009.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-2, 9-13, 16-17, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laxmi et al. ("Performance Analysis of FFT Algorithms on Multiprocessor Systems") in view of Chu et al. ("Inside the FFT Black Box: Serial and Parallel Fast Fourier Transform Algorithms").

Re claim 1, Laxmi et al. disclose in pages 512-521 a method for controlling processing elements in a multiprocessor architecture to provide improve throughput for FFT/IFFT computations (e.g. introduction section in page 512), the method comprising the steps of: computing, on a multiprocessor architecture including "P" processing elements (e.g. Figure 1), each butterfly of the first "log.sub.2P" stages of an FFT/IFFT on either a single one of the processing elements or on each of the "P" processing elements

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simultaneously (e.g. Figure 2, wherein  $P = N/P$  as seen in section II "Radix-2 FFT computation" in right column page 513, particularly step 1), and distributing the computation of the butterflies in all the subsequent stages of the FFT/IFFT among the "P" processing elements such that each chain of cascaded butterflies consisting of those butterflies that have inputs and outputs connected together, are processed by the same processing element (e.g. Figure 2, section II "Radix-2 FFT computation" in right column page 513, particularly steps 2-3).

Laxmi et al. do not explicitly disclose the limitation of thereby eliminate the need for inter-processor communication after the computation of the first "log.sub.2P" stages. However, Chu et al. disclose an architecture of performing FFT which eliminate the need for inter-processor communication after the computation of the first "log.sub.2P" stages (e.g. chapters 17 and 19, particularly page 191 in the introduction section).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the limitation of eliminating the need for inter-processor communication after the computation of the first "log.sub.2P" stages as reasonably seen in Chu et al.'s invention into Laxmi et al.'s invention because it would enable to enhance the system performance by parallel processing.

Re claim 2, Laxmi et al. further disclose in pages 512-521 the distributing of the computation of the butterflies subsequent to the first "log.sub.2P" butterflies is achieved by assigning operand addresses of each set of butterfly operands to each processing element in such a manner that the butterfly is processed by the same processing element that computed the connected butterfly of the previous stage in the same chain of

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butterflies (e.g. Figure 2, section II “Radix-2 FFT computation” in right column page 513, particularly steps 2-3 and first paragraph of right column in page 514).

Re claim 9, it has similar limitations cited in claim 1. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 10, Laxmi et al. further disclose in pages 512-521 the first  $\log_2(P)$  stages of the transform are calculated on all of the processors operating in parallel (e.g. Figure 2 and first paragraph of right column in page 514).

Re claim 11, Laxmi et al. further disclose in pages 512-521 the method is performed on two processors (e.g. last paragraph left column and first paragraph right column in page 514 wherein  $P = 2$ ), and wherein the first two stages of a radix-2 fast Fourier transform or inverse fast Fourier transform are calculated, and wherein the subsequent stages of the transform are computed as radix-2 stages (e.g. Figure 2 as radix-2). Laxmi et al. fail to disclose in pages 512-521 the first two radix-2 can be performed as radix-4. However, the implementation logically and mathematically of radix-4 as two radix-2 or vice versa is well known in the art of technology and widely used. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the two radix-2 as one radix-4 into Laxmi et al.’s invention because it would enable to increase the system performance by operating the radix-4 in single unit.

Re claim 12, Laxmi et al. further disclose in pages 512-521 chains comprises a single loop that iterates  $N/2 * (\log_2(N/2)) / (\text{number of processors})$  times (e.g. Figure 2 and step 3 in the last paragraph right column in page 513).

Re claim 13, Laxmi et al. further disclose in pages 512-521 each butterfly computational block includes a plurality of operands each having an associated address (e.g. fetching data from storage), and wherein calculating chains of butterfly computational blocks corresponding to the subsequent stages comprises assigning addresses to each of the operands so that each butterfly block in a chain is calculated in the same processor (e.g. Figure 2).

Re claim 16, Laxmi et al. disclose in pages 512-521 a processor system, comprising: a memory operable to store samples of an input signal (e.g. M boxes in Figure 1a); a plurality of processors couple to the memory (e.g. P boxes in Figure 1a), the plurality of processors operable to receive the samples from the memory and to use the samples to execute to the butterfly computational blocks for the first "log.sub.2P" stages of a fast Fourier transform or inverse Fast Fourier on either a single one of the processors or on a plurality of the processors operating in parallel (e.g. Figure 2, wherein  $P = N/P$  as seen in section II "Radix-2 FFT computation" in right column page 513, particularly step 1); and address circuitry coupled to the memory and processor and operable to distribute the computation of the butterfly computational blocks in all stages subsequent to the first log.sub.2P states among the plurality of processors such that each chain of cascaded butterfly computational blocks in the transform are coupled in series and are computed by the same processor (e.g. Figure 2, section II "Radix-2 FFT computation" in right column page 513, particularly steps 2-3).

Laxmi et al. do not explicitly disclose the limitation of thereby eliminate the need for inter-processor communication after the computation of the first "log.sub.2P" stages.

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However, Chu et al. disclose an architecture of performing FFT which eliminate the need for inter-processor communication after the computation of the first "log.sub.2P" stages (e.g. chapters 17 and 19, particularly page 191 in the introduction section).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the limitation of eliminating the need for inter-processor communication after the computation of the first "log.sub.2P" stages as reasonably seen in Chu et al.'s invention into Laxmi et al.'s invention because it would enable to enhance the system performance by parallel processing.

Re claim 17, it has similar limitations cited in claim 13. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 20, Laxmi et al. further disclose in pages 512-521 each of the processors comprises a digital signal processor (e.g. introduction section in page 512).

Re claim 21, it has similar limitations cited in claim 16. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 22, Laxmi et al. further disclose in pages 512-521 the electronic system comprises a communications system (e.g. abstract and introduction sections in page 512).

Re claim 23, it has similar limitations cited in claim 20. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

#### ***Allowable Subject Matter***

5. Claims 5-8 are allowed.

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6. Claims 3-4, 14-15 and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Response to Arguments***

7. Applicant's arguments with respect to claims 1-2, 9-13, 16-17, and 20-23 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/  
Primary Examiner, Art Unit 2193

August 31, 2009